What is claimed is:

1. A method for generating a delay time comprising:

determining a number of loops value associated with a delay time and at least one characteristic value associated with a counter;

determining a remaining count value based on the number of loops value; and

generating the delay time with the counter based on the number of loops value and the remaining count value.

2. A method as defined in claim 1, further comprising obtaining a current count value and performing a comparison based on the current count value and a previous count value at least a number of times equal to the number of loops value.

3. A method as defined in claim 2, further comprising determine that the delay time has been reached based on the comparison.

4. A method as defined in claim 2, wherein obtaining the current count value comprises reading a running count value of the counter.

5. A method as defined in claim 1, further comprising obtaining an initial count value.

6. A method as defined in claim 5, wherein determining the number of loops value comprises determining the number of loops value based on at least the initial count value.

7. A method as defined in claim 5, wherein determining the remaining count value comprises determining the remaining count value based on at least the initial count value.

8. A method as defined in claim 1, further comprising polling the counter.

9. A method as defined in claim 8, wherein polling the counter comprises polling the counter in a non-interrupt environment.

10. A method as defined in claim 1, wherein determining the number of loops value includes determining a number of rollover events to be generated by the counter.

11. A method as defined in claim 1, wherein generating the delay time comprises generating the delay time prior to a boot process.

12. An apparatus for generating a delay time comprising:

a processor system including a memory;

instructions stored in the memory that enable the processor system to:

determine a number of loops value associated with a delay time and at least one characteristic value associated with a counter;

determine a remaining count value based on the number of loops value; and

generate the delay time with the counter based on the number of loops value and the remaining count value.

13. An apparatus as defined in claim 12, wherein the instructions stored in the memory enable the processor system to obtain a current count value and perform a comparison based on the current count value and a previous count value at least a number of times equal to the number of loops value.

14. An apparatus as defined in claim 13, wherein the instructions stored in the memory enable the processor system to determine that the delay time has been reached based on the comparison.

15. An apparatus as defined in claim 12, wherein the instructions stored in the memory enable the processor system to obtain an initial count value.

16. An apparatus as defined in claim 15, wherein the instructions stored in the memory enable the processor system to determine the number of loops value based on at least the initial count value.

17. An apparatus as defined in claim 12, wherein the instructions enable the processor system to poll the counter in a non-interrupt environment.

18. An apparatus as defined in claim 12, wherein the instructions enable the processor system to determine a number of rollover events to be generated based on the number of loops value.

19. An apparatus as defined in claim 12, wherein the instructions enable the processor system to generate the delay time prior to a boot process.

20. An apparatus as defined in claim 12, wherein the memory is at least one of a flash memory and a read only memory.

21. A system for generating a delay time comprising:

a count reader configured to obtain count values from a counter;

a comparator communicatively coupled to the count reader and configured to perform comparisons based on at least some of the count values;

a loop counter communicatively coupled to the comparator and configured to modify a number of loops value based on at least some of the comparisons, wherein the system generates a delay time based on the comparisons, the number of loops value, and a remaining count value.

22. A system as defined in claim 21, wherein the count reader is configured to obtain an initial count value.

23. A system as defined in claim 22, further comprising a value generator that is configured to generate the remaining count value and the number of loops value based on the initial count value.

24. A system as defined in claim 21, wherein the at least some of the count values include at least one of a previous count value and a current count value.

25. A system as defined in claim 24, wherein the comparator performs the comparisons based on at least one of the previous count value and the current count value.

26. A system as defined in claim 21, wherein the counter is at least one of a non-resetable counter and non-resetable timer.

27. A system as defined in claim 21, wherein the system generates the delay time in a non-interrupt environment.

28. A system as defined in claim 21, wherein the system generates the delay time prior to a boot phase.

29. A computer readable medium having instructions stored thereon that, when executed, cause a machine to:

determine a number of loops value associated with a delay time and at least one characteristic value associated with a counter;

determine a remaining count value based on the number of loops value; and

generate the delay time with the counter based on the number of loops value and the remaining count value.

30. A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to obtain a current count value and perform a comparison based on the current count value and a previous count value at least a number of times equal to the number of loops value.

31. A computer readable medium as defined in claim 30 having instructions stored thereon that, when executed, cause the machine to determine that the delay time has been reached based on the comparison.

32. A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to obtain an initial count value.

33. A computer readable medium as defined in claim 32 having instructions stored thereon that, when executed, cause the machine to determine the number of loops value based on at least the initial count value.

34. A computer readable medium as defined in claim 32 having instructions stored thereon that, when executed, cause the machine to determine the remaining count value based on at least the initial count value.

35. A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to poll the counter.

36. A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to poll the counter in a non-interrupt environment.

37. A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to decrement the number of loops value based on at least one rollover event of the counter.

38. A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to generate the delay time prior to a boot process.

39. An apparatus for generating a delay time comprising:

a processor system including a flash memory;

instructions stored in the flash memory that enable the processor system to:

determine a number of loops value associated with a delay time and at least one characteristic value associated with a counter;

determine a remaining count value based on the number of loops value; and

generate the delay time with the counter based on the number of loops value and the remaining count value.

40. An apparatus as defined in claim 39, wherein the instructions enable the processor system to generate the delay time prior to a boot process.